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Line Output Improvement by Diminishing Waste Process

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***Abstract*-Improving efficiency of existing material can be obtained only if the existing workforce spends their time on value added services. For this the concept of motion study is utilized by which we can determine the operator efficiency and can use the data to produce rational and reasonable results. The status of machines are obtained to find out the amount of production and the wastage in resources.TR in pocket fail check has also been done to verify the procedure employed by operators in case of TR in pocket fail error.LOT PROCESSING involves following a lot from the time of entry to testing to the stage of getting reeled. For gravity handlers the times taken for each steps in processing of a lot are calculated and time periods of each are compared and top errors are tackled. For SRM HANDLERS the frequencies of errors are measured and the errors with high frequencies are minimized. SETUP STUDY has also been done as part of the program in which the time taken for different steps in setup is calculated and the non value adding time is reduced. By doing setup study and lot processing the production rate can be improved by diminishing time wasters and reducing high frequency errors. However all said it would a futile attempt not to provide any solutions to the data analyzed by the above method. With respect to the company's functioning, feasibility and resources available solutions have been provided to the problems that were identified. The production is expected to rise with implementation of these solutions.**

***Index Terms*-- lot processing, setup study,SRM handlers**

I. INTRODUCTION

Semiconductor devices are electronic components that are invented to exploit the most electronic properties of semiconductor materials which among are principally silicon, germanium, and gallium arsenide, as well as organic semiconductors. Semiconductor devices have replaced thermionic devices (vacuum tubes) inmost applications most applications. They use electronic conduction in the solid state as opposed to the gaseous state or thermionic emission in a high vacuum. The manufacturing of IC takes place in below steps.

II. FRONT-END-OF-LINE (FEOL) PROCESSING

FEOL processing refers to the formation of the transistors directly in the silicon. The raw wafer is engineered by the growth of an ultrapure, virtually defect-free silicon layer through epitaxy. In the most advanced logic devices, prior to the silicon epitaxy step, tricks are performed to improve the performance of the transistors to be built. One method involves introducing a straining step wherein a silicon variant such as silicon-germanium (SiGe) is deposited. Once the epitaxial silicon is deposited, the crystal lattice becomes stretched somewhat, resulting in improved electronic mobility. Another method, called silicon on insulator technology involves the insertion of an insulating layer between the raw silicon wafer and the thin layer of subsequent silicon epitaxy. This method results in the creation of transistors with reduced parasitic effects.

Gate Oxide and Implants: Front-end surface engineering is followed by growth of the gate dielectric, traditionally silicon dioxide (SiO_2), patterning of the gate, patterning of the source and drain regions, and subsequent implantation or diffusion of dopants to obtain the desired complementary electrical properties. In dynamic random access memory (DRAM) devices, storage capacitors are also fabricated at this time typically stacked above the access transistor.

Die Preparation**:** Die preparation is a step of semiconductor device fabrication during which a wafer is prepared for IC packaging and IC testing. The process of die preparation typically consists of 2 steps: wafer mounting and wafer dicing.

III. BACK-END-OF-LINE (BEOL) PROCESSING METAL LAYERS

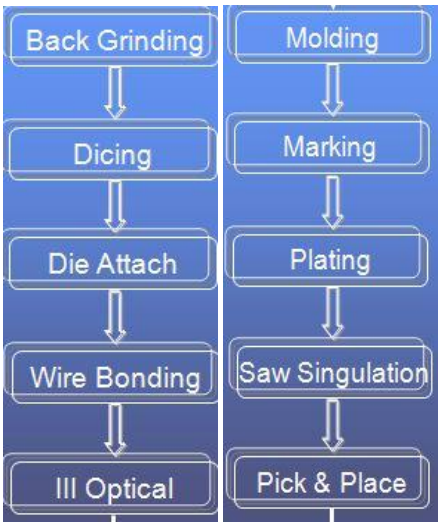
Once the various semiconductor devices have been created, they must be interconnected to form the desired electrical circuits. This occurs in a series of wafer processing steps collectively referred to as BEOL (not to be confused with back end of chip fabrication which refers to the packaging and testing stages). BEOL processing involves creating metal interconnecting wires that are isolated by dielectric layers. The insulating material was traditionally a form of SiO_2 or a silicate glass, but recently new low dielectric constant materials are being used. These dielectrics presently take the form of SiOC (silicon oxycarbide) and have dielectric constants around 2.7 (compared to 3.9 for SiO_2), although materials with constants as low as 2.2 are being offered to chipmakers.

INTERCONNECT: Historically, the metal wires consisted of aluminum. In this approach to wiring often called subtractive aluminum, blanket films of aluminum are deposited first, patterned, and then etched, leaving isolated wires. Dielectric material is then deposited over the exposed wires. The various metal layers are interconnected by etching holes, called vias, in the insulating material and depositing tungsten in them with a CVD technique. This approach is still used in the

fabrication of many memory chips such as dynamic random access memory (DRAM) as the number of interconnect levels is small, currently no more than four. More recently, as the number of interconnect levels for logic has substantially increased due to the large number of transistors that are now interconnected in a modern microprocessor, the timing delay in the wiring has become significant prompting a change in wiring material from aluminum to copper and from the silicon dioxides to newer low-K material. This performance enhancement also comes at a reduced cost via damascene processing that eliminates processing steps. As the number of interconnect levels increases, planarization of the previous layers is required to ensure a flat surface prior to subsequent lithography. Without it, the levels would become increasingly crooked and extend outside the depth of focus of available lithography, interfering with the ability to pattern. CMP (chemical-mechanical planarization) is the primary processing method to achieve such planarization although dry etch back is still sometimes employed if the number of interconnect levels is no more than three.

WAFER MOUNTING: Wafer mounting is a step that is performed during the die preparation of a wafer as part of the process of semiconductor fabrication. During this step, the wafer is mounted on a plastic tape that is attached to a ring. Wafer mounting is performed right before the wafer is cut into separate dies. The adhesive film on which the wafer is mounted ensures that the individual dies remain firmly in place during 'dicing', as the process of cutting the wafer is called. The picture on the right shows a 300 mm wafer after it was mounted and diced. The blue plastic is the adhesive tape. The wafer is the round disc in the middle. In this case, a large number of dies were already removed.

SEMICONDUCTOR-DIE CUTTING: In the manufacturing of micro-electronic devices, die cutting, dicing or singulation is a process of reducing a wafer containing multiple identical integrated circuits to individual dies each containing one of those circuits. During this process, a wafer with up to thousands of circuits is cut into rectangular pieces, each called a die. In between those functional parts of the circuits, a thin non-functional spacing is foreseen where a saw can safely cut the wafer without damaging the circuits. This spacing is called scribe line or saw street. The width of the scribe is very small, typically around 100 µm. A very thin and accurate saw is therefore needed to cut the wafer into pieces. Usually the dicing is performed with a water-cooled circular saw with diamond-tipped teeth. After the die is manufactured they are made in to IC's by IC assembly and they are later tested. The flow chart of IC testing is give below.



IV. TESTING

Once the front-end process has been completed, the semiconductor devices are subjected to a variety of electrical tests to determine if they function properly. The proportion of devices on the wafer found to perform properly is referred to as the yield.

WAFER TEST: The highly serialized nature of wafer processing has increased the demand for metrology in between the various processing steps. Wafer test metrology equipment is used to verify that the wafers haven't been damaged by previous processing steps up until testing. If the number of dies—the integrated circuits that will eventually become chips— etched on a wafer exceeds a failure threshold (i.e. too many failed dies on one wafer), the wafer is scrapped rather than investing in further processing.

DEVICE TEST: Once the front-end process has been completed, the semiconductor devices are subjected to a variety of electrical tests to determine if they function properly. The proportion of devices on the wafer found to perform properly is referred to as the yield. The fab tests the chips on the wafer with an electronic tester that presses tiny probes against the chip. The machine marks each bad chip with a drop of dye. Currently, electronic dye marking is possible if wafer test data is logged into a central computer database and chips are "binned" (i.e. sorted into virtual bins) according to predetermined test limits. The resulting binning data can be graphed, or logged, on a wafer map to trace manufacturing defects and mark bad chips. This map can be also used during wafer assembly and packaging.

V. TASK DONE

As earlier we saw for lot processing we are reducing the time taken to finish a lot. But before that conversion of handler and setup of tester takes place. If there is a change in package type of IC we perform handler conversion followed by setup. If there is a change in device type we install the new setup. The study of processes that takes place during the setup is called setup study. Here we note down the time taken for each step of setup process by following many setup's and then try to reduce the overall time taken. The setup study is again done both on gravity handlers as well as SRM handlers: The time frame analysis for gravity handlers involves dividing the setup time into value added and non value added times. The study is conducted on a large scale to avoid randomness.

The time frame graph for gravity handlers:

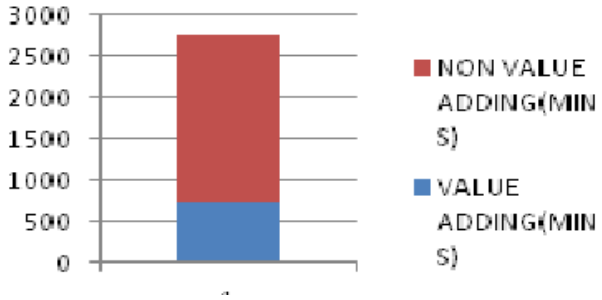


Fig. 1: Time Frame Analysis Gravity Handler

The tabular collection of various time wasters:

FACTORS	TIME	%	CUMULATIV
CONVERSION AFTER WORK ORDER	470	22.11	22.11
VOUT FAIL PROBLEM	300	14.11	36.23
PRODUCTION START AFTER SET UP	285	13.411	49.64
HANDLER PROBLEM IN CONVERSION	220	10.35	60
HANDLER LEFT IDLE AS IT WAS FOUND DEVICE WONT RUN IN THE HANDLER	200	9.41	69.41
TIME TAKEN FOR 1ST AND SECOND SETUP	180	8.47	77.88
TIME TAKEN FOR HANDLER TO CHANGE AND PRODUCTION TO START	180	8.47	86.35
SET UP START AFTER CONVERSION	130	6.11	92.47
ATTENDING OTHER HANDLER	80	3.76	96.23
MACHINE IDLE FOR NO REASON	35	1.64	97.88
CONVERSION TIME	25	1.17	99.05
WAIT FOR TOOLS(BOLTS)	20	0.94	100
TOTAL	2125		

Using the above the pareto chart has been drawn. The pareto chart analysis and various time wasters for gravity handlers are:

The pareto chart [1] for set up study is:

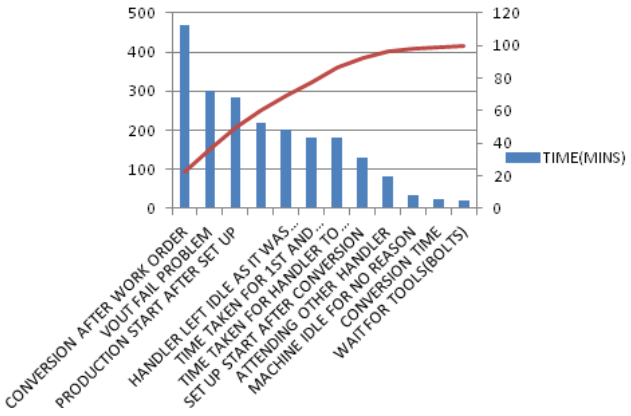


Fig. 2: Pareto chart analysis for gravity handler

For SRM HANDLERS the set up non value adding and value adding time(MINS) are differentiated as:

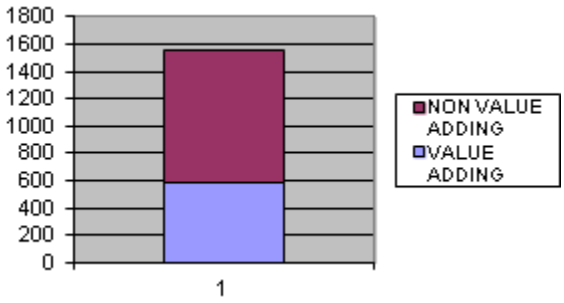


Fig. 3: Time Frame Analysis SRM Handler

The tabular collection of various time wasters (in MINS) in SRM handlers:

FACTORS	TIME	%	cumulative
TEST SITE CALLIBRATION	250	26.31	26.31
QC TEST AFTER SETUP	225	23.68	50
ATTENDING OTHER HANDLER	170	17.89	67.89
WORK TO START AFTER ORDER	115	12.10	80
WAITING FOR TOOLS	105	11.05	91.05
MACHINE IDLE FOR NO REASON	85	8.94	100
total	950		

The pareto chart[2] for set up study in SRM handlers:

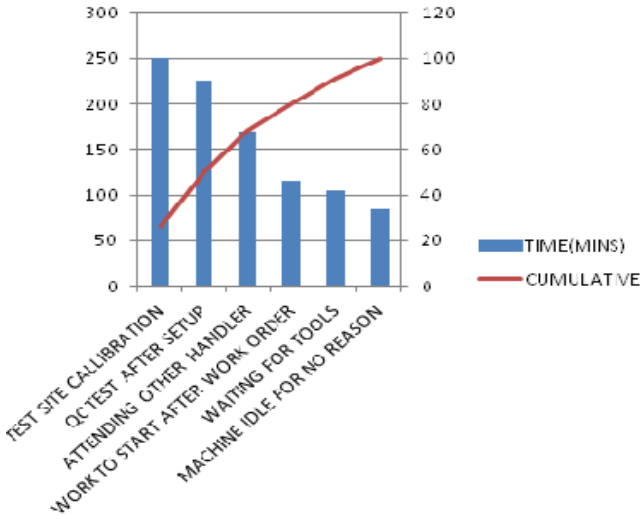


Fig. 4: Pareto chart analysis for SRM handler

Here we try to give solutions to top three errors in both SRM and GRAVITY handlers.

VI. Solutions Provided

SRM SET UP STUDY:

- **Dedicated setup's are must to decrease the number of set up's**
- **By dedicated setups online problems also will be reduced as the handler will be fine tuned.**

Task assigned: To reduce the below time wasters in SRM HANDLERS

- Test site calibration
- QC test after setup
- Attending other handlers
- Work to start after work order

Action to be Taken :

Problem # 1:

Test site calibration

- The tester resources and parts shall not disturbed.
- After completion of setup if the devices are failing frequently, we have to check for alignment issues, cable connectivity problems, program error before doing calibration.
- The condition of test site can be verified first before embarking on setup so that calibration after setup can be avoided and wastage of handler time be prevented.
- Test site calibration can be done at idle time of tester or at the time of conversion

Problem # 2:

QC checks AFTER SETUP:

Action to be taken:

- The QC checking parameters like package size, reel size etc., can be verified parallel to set up.
- Awareness about idle time must be created so that QC attends machine immediately after completion of set up
- The setup personal must immediately inform QC about completion of set up

Problem # 3:

ATTENDING ANOTHER HANDLER:

Action to be Taken:

- Much time shall not be wasted for attending another handler.
- Increase in man power.

Problem # 4:

WORK TO START AFTER WORK ORDER

Action to be taken:

Shift in charge shall immediately inform ENGINEERING DEPARMENT about the set up

Gravity handlers SET UP STUDY:

Task assigned: To reduce the below time wasters:

- Conversion after work order
- Vout fail problem
- Production to start after setup

Problem # 1:

WORK TO START AFTER WORK ORDER

Action to be taken:

Shift in charge shall immediately inform maintenance personal about conversion.

Target Improvement: unwanted time waste can be reduced.

Problem # 3: Vout fail problem.

Action to be taken: Aged devices must be replaced time to time.

Target Improvement: unwanted time waste can be reduced.

Problem # 2:Production to start after setup

Action to be taken: Operator shall be immediately assigned after completion of set up.Effective planning shall be done.

Target Improvement: unwanted time waste can be reduced. Wastage of time at completion and start of the shift must be avoided. However more erroneous errors such as double time setup, faulty handler choice must be avoided.

VII. LIMITATIONS

This division of value adding and non value adding steps/time and providing solutions is one face of the coin while the real challenge would be bring out radical change in the equipment and software used. While financial constraints are present, making changes in hard ware design or software code of SRM HANDLER is impossible. Frequently occurring errors in SRM HANDLERS are avoided fine tuning handlers over a period of time. This may take long time and manual disturbances to machine also affect the fine tuning process. So mechanical addititonalities shall be made to avoid those frequently occurring errors. This is a difficult task in this case.

CONCLUSION

Testing being a major process in semiconductor field must be carefully done without erroneous time wasters. The ergonomics study helped in differentiating the value added and non-value added times improving the efficiency with the present work force. The LOT PROCESSING and SET UP STUDY have the potential of reducing the time wasters and improving the production. The method followed in the project is that of DMAIC.in which we first DEFINE the problem. Then MEASURE, collect the data then ANALYZE, IMPROVE and CONTROL the problem. This a six sigma method of solving a problem. This technique finds its use in many industries for reducing the wastage time

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